Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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ANALOG DEVICES

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Editors' Notes

40TH ANNIVERSARY

We're still celebrating the 40th anniversary of Analog Devices, Inc. Such events create a temptation to wax historical, and this is no exception. If you're interested in the high points of our history, the spread on pages 10-11 depicts the contents page of a timeline accessible on the Web (www.analog.com/timeline); in it you can click on any year to access a brief audiovisual clip reviewing that year's major corporate events.

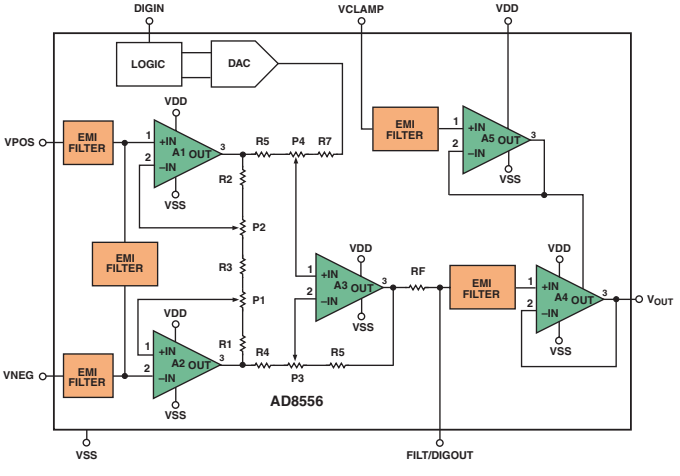
As part of the celebration, we've devoted this year's four print issues to articles with principal technological focus on (1) digital, (2) conversion, (3) analog, and (4) sensors. This issue is devoted to articles discussing aspects of *analog* technology. As you will see, even digital phenomena are analog at the hardware level.

RFI AGAIN—GONE!

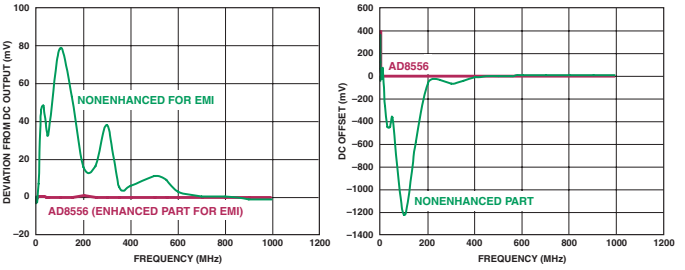
On multiple occasions, we've referred to—or had our attention called to—the dc offset problems caused by common-mode RF interference with low-frequency measurements, particularly as manifested by rectification in the input stages of instrumentation amplifiers.[1,2,3]

Our purpose for bringing this subject up again is to mention the availability, since July 2005, of a digitally programmable instrumentation amplifier that contains an intrinsic solution to the problem. The AD8556,[4] designed for automotive and industrial applications, features internal electromagnetic-interference (EMI) filtering; in addition, it has a very wide temperature range, low-offset voltage and drift, and open- and shorted-wire protection. It can provide a complete signal processing path from a bridge sensor to an A/D converter. Typical applications are with pressure sensors in anti-lock brake systems (ABS), occupant detection systems, fuel level sensors, transmission controls, and precision strain or pressure gauges.

The figure below shows where the on-chip EMI filters are applied to protect the device's inputs: at the main differential inputs, at the *clamp* input, and at the input of the output amplifier. In brief, the problem that they solve is to filter out high frequencies before they reach the amplifier input junctions and create dc offsets through partial rectification.[5]



The effectiveness of this filtering scheme can be seen in the figures at the top of next column, comparing responses of the AD8556 and the AD8555, a similar device—but without internal EMI protection. The graph at left compares their dc responses to 200-mV common-mode high-frequency signals that drive both differential inputs (G = 70 mV/mV). The one at right measures dc output responses to 200-mV p-p of high-frequency sine waves driving VPOS, with VNEG grounded.



More about the AD8556: specified with 10-µV max offset voltage, 65-nV/°C max offset drift, and 112-dB typical common-mode rejection, it features digitally programmable gain (from 70 mV/mV to 1280 mV/mV) and output-offset voltage, open- and short-circuited-wire fault detection, low-pass filtering, EMI filtering, and output voltage clamping. Output offset voltage can be adjusted with 0.39% resolution. Gain and offset can be temporarily programmed by the user and evaluated in-circuit, then permanently programmed by blowing polysilicon fuse links. The AD8556 operates on a single 2.7-V to 5.5-V supply and consumes 2 mA. Specified from –40°C to +140°C, it is available in 8-lead SOIC and 16-lead, 3-mm × 3-mm LFCSP packages.

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[1] "Ask The Applications Engineer—14" http://www.analog.com/library/analogdialogue/Anniversary/14.html *Ask The Applications Engineer*, Analog Devices http://www.analog.com/library/analogdialogue/Anniversary/contents.html

[2] "A Reader Notes" http://www.analog.com/library/analogdialogue/Anniversary/Reader_Notes.html

[3] H.R. Gelbach, "A Reader Notes: High-Frequency-Caused Errors in Millivolt Measurement Systems," *Analog Dialogue* 37-3, 2003, pp. 2, 14. http://www.analog.com/library/analogdialogue/archives/issues/vol37n3.pdf

[4] http://www.analog.com, Search <AD8556>

[5] W. Jung, ed., "*Op Amp Applications Handbook*", Elsevier-Newnes, 2005, pp. 719-726. Similar material can be found online in the Analog Devices seminar version, http://www.analog.com/library/analogdialogue/archives/39-05/Web_Ch7_final_J.pdf, pp. 7.122-7.129.

THE ANALOG WORLD

In mixed-signal systems, an analog-to-digital converter (ADC) translates real-world analog signals into the digital domain so that further signal processing can be implemented by the DSP or embedded processor. A digital-to-analog converter (DAC) then translates the digital signals back into the analog domain. At the start of the chain, and at the end of the day, the signals that we transmit, measure, and control are analog: audio, video, temperature, pressure, voltage, and current, for instance.

Some amount of analog signal conditioning is always required before the ADC and after the DAC. Even functions that may at first appear to be digital are often analog at their very heart. Take phased-lock loops (PLLs), for example. These include phase detectors, filters, and oscillators—all analog functions. Direct digital synthesis (DDS) devices, on the other hand, are mostly digital, but they provide output signals whose properties are measured using analog quantities such as phase, frequency, and amplitude.

When designing analog circuitry—especially where high speed, high resolution, or low noise is required—a good printed-circuit board layout becomes increasingly important. Careful attention to voltage levels and signal flow can minimize the need for an expensive, time-consuming redesign, and can maintain optimum performance throughout the signal path.

With all this in mind, we invite you to read the "analog" installment of *Analog Dialogue*'s tribute to ADI's 40th anniversary. Here you will learn about adding stereo audio to a low-cost satellite set-top box; using DDS to generate waveforms for test, measurement, and communications; and avoiding the layout pitfalls inherent in high-speed amplifier designs. Enjoy!

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A Practical Guide to High-Speed Printed-Circuit-Board Layout

By John Ardizzoni [john.ardizzoni@analog.com]

Despite its critical nature in high-speed circuitry, printed-circuit-board (PCB) layout is often one of the last steps in the design process. There are many aspects to high-speed PCB layout; volumes have been written on the subject. This article addresses high-speed layout from a practical perspective. A major aim is to help sensitize newcomers to the many and various considerations they need to address when designing board layouts for high-speed circuitry. But it is also intended as a refresher to benefit those who have been away from board layout for a while. Not every topic can be covered in detail in the space available here, but we address key areas that can have the greatest payoff in improving circuit performance, reducing design time, and minimizing time-consuming revisions.

Although the focus is on circuits involving high-speed op amps, the topics and techniques discussed here are generally applicable to layout of most other high-speed analog circuits. When op amps operate at high RF frequencies, circuit performance is heavily dependent on the board layout. A high-performance circuit design that looks good "on paper" can render mediocre performance when hampered by a careless or sloppy layout. Thinking ahead and paying attention to salient details throughout the layout process will help ensure that the circuit performs as expected.

The Schematic

Although there is no guarantee, a good layout starts with a good schematic. Be thoughtful and generous when drawing a schematic, and think about signal flow through the circuit. A schematic that has a natural and steady flow from left to right will tend to have a good flow on the board as well. Put as much useful information on the schematic as possible. The designers, technicians, and engineers who will work on this job will be most appreciative, including us; at times we are asked by customers to help with a circuit because the designer is no longer there.

What kind of information belongs on a schematic besides the usual reference designators, power dissipations, and tolerances? Here are a few suggestions that can turn an ordinary schematic into a *super*schematic! Add waveforms, mechanical information about the housing or enclosure, trace lengths, keep-out areas; designate which components need to be on top of the board; include tuning information, component value ranges, thermal information, controlled impedance lines, notes, brief circuit operating descriptions … (and the list goes on).

Trust No One

If you're not doing your own layout, be sure to set aside ample time to go through the design with the layout person. An ounce of prevention at this point is worth more than a pound of cure! Don't expect the layout person to be able to read your mind. Your inputs and guidance are most critical at the beginning of the layout process. The more information you can provide, and the more involved you are throughout the layout process, the better the board will turn out. Give the designer interim completion points—at which you want to be notified of the layout progress for a quick review. This "loop closure" prevents a layout from going too far astray and will minimize reworking the board layout.

Your instructions for the designer should include: a brief description of the circuit's functions; a sketch of the board that shows the input and output locations; the board *stack up* (i.e., how thick the board will be, how many layers, details of signal layers and planes—power, ground, analog, digital, and RF); which signals need to be on each layer; where the critical components need to be located; the exact location of bypassing components; which traces are critical; which lines need to be controlled-impedance lines; which lines need to have matched lengths; component sizes; which traces need to kept away from (or near) each other; which *circuits* need to be kept away from (or near) each other; which *components* need to be close to (or away from) each other; which components go on the top and the bottom of the board. You'll never get a complaint for giving someone too much information—too *little*, yes; too much, no.

> *A learning experience:* About 10 years ago I designed a multilayer surface-mounted board—with components on both sides of the board. The board was screwed into a gold-plated aluminum housing with many screws (because of a stringent vibration spec). Bias feedthrough pins poked up through the board. The pins were wire-bonded to the PCB. It was a complicated assembly. Some of the components on the board were to be *SAT* (set at test). But I hadn't specified where these components should be. Can you guess where some of them were placed? Right! On the bottom of the board. The production engineers and technicians were not very happy when they had to tear the assembly apart, set the values, and then reassemble everything. I didn't make that mistake again.

Location, Location, Location

As in real estate, location is everything. Where a circuit is placed on a board, where the individual circuit components are located, and what other circuits are in the neighborhood are all critical.

Typically, input-, output-, and power locations are defined, but what goes on between them is "up for grabs." This is where paying attention to the layout details will yield significant returns. Start with critical component placement, in terms of both individual circuits and the entire board. Specifying the critical component locations and signal routing paths from the beginning helps ensure that the design will work the way it's intended to. Getting it right the first time lowers cost and stress—and reduces cycle time.

Power-Supply Bypassing

Bypassing the power supply at the amplifier's supply terminals to minimize noise is a critical aspect of the PCB design process—both for high-speed op amps and any other high-speed circuitry. There are two commonly used configurations for bypassing high-speed op amps.

Rails to ground: This technique, which works best in most cases, uses multiple parallel capacitors connected from the op amp's power-supply pins directly to ground. Typically, two parallel capacitors are sufficient—but some circuits may benefit from additional capacitors in parallel.

Paralleling different capacitor values helps ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is especially important at frequencies where the op amp *power-supply rejection* (PSR) is rolling off. The capacitors help compensate for the amplifier's decreasing PSR. Maintaining a low impedance path to ground for many decades of frequency will help ensure that unwanted noise doesn't find its way into the op amp. Figure 1 shows the benefits of multiple parallel capacitors. At lower frequencies the larger capacitors offer a low impedance path to ground. Once those capacitors reach self resonance, the capacitive quality diminishes and the capacitors become inductive. That is why it is important to use multiple capacitors: when one capacitor's frequency response is rolling off, another is becoming significant, thereby maintaining a low ac impedance over many decades of frequency.

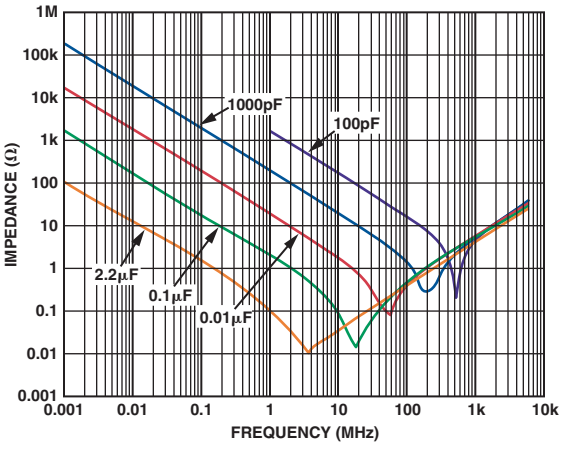

Figure 1. Capacitor impedance vs. frequency.

Starting directly at the op amp's power-supply pins; the capacitor with the lowest value and smallest physical size should be placed on the same side of the board as the op amp—and as close to the amplifier as possible. The ground side of the capacitor should be connected into the ground plane with minimal lead- or trace length. This ground connection should be as close as possible to the amplifier's load to minimize disturbances between the rails and ground. Figure 2 illustrates this technique.

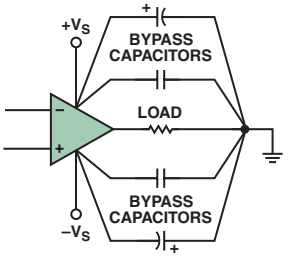

Figure 2. Parallel-capacitor rails-to-ground bypassing.

This process should be repeated for the next-higher-value capacitor. A good place to start is with 0.01 µF for the smallest value, and a 2.2-µF—or larger—electrolytic with low ESR for the next capacitor. The 0.01 µF in the 0508 case size offers low series inductance and excellent high-frequency performance.

Rail to rail: An alternate configuration uses one or more bypass capacitors tied between the positive- and negative supply rails of the op amp. This method is typically used when it is difficult to get all four capacitors in the circuit. A drawback to this approach is that the capacitor case size can become larger, because the voltage across the capacitor is double that of the single-supply bypassing method. The higher voltage requires a higher breakdown rating, which translates into a larger case size. This option can, however, offer improvements to both PSR and distortion performance.

Since each circuit and layout is different; the configuration, number, and values of the capacitors are determined by the actual circuit requirements.

Parasitics

Parasitics are those nasty little gremlins that creep into your PCB (quite literally) and wreak havoc within your circuit. They are the hidden stray capacitors and inductors that infiltrate high-speed circuits. They include inductors formed by package leads and excess trace lengths; pad-to-ground, pad-to-power-plane, and pad-to-trace capacitors; interactions with vias, and many more possibilities. Figure 3(a) is a typical schematic of a noninverting op amp. If parasitic elements were to be taken into account, however, the same circuit would look like Figure 3(b).

In high-speed circuits, it doesn't take much to influence circuit performance. Sometimes just a few tenths of a picofarad is enough. Case in point: if only 1 pF of additional stray parasitic capacitance is present at the inverting input, it can cause almost 2 dB of peaking in the frequency domain (Figure 4). If enough capacitance is present, it can cause instability and oscillations.

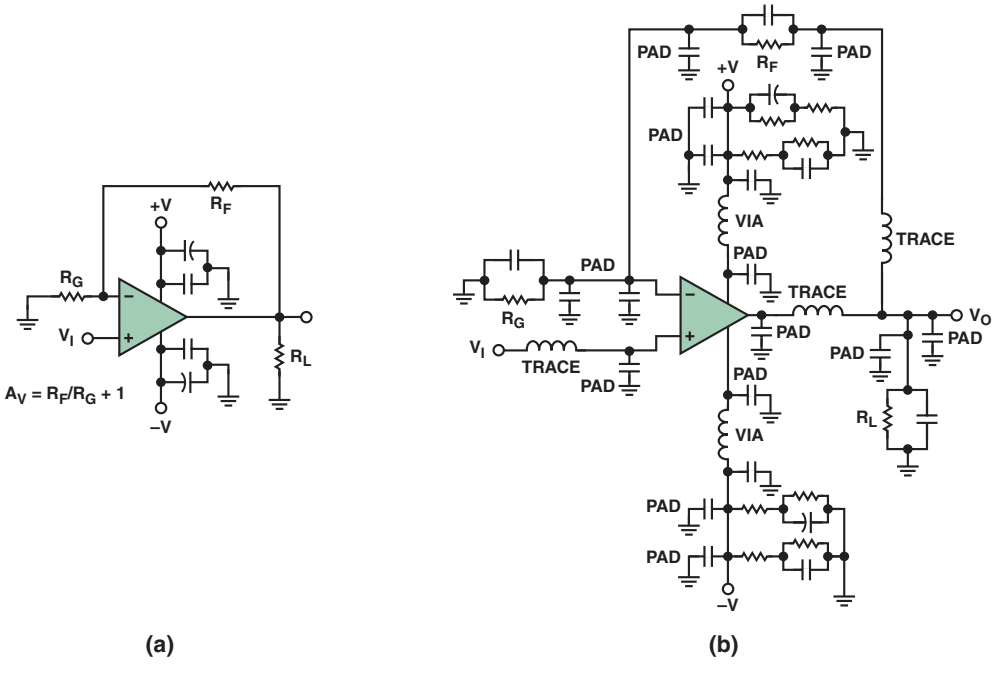

Figure 3. Typical op amp circuit, as designed (a) and with parasitics (b).

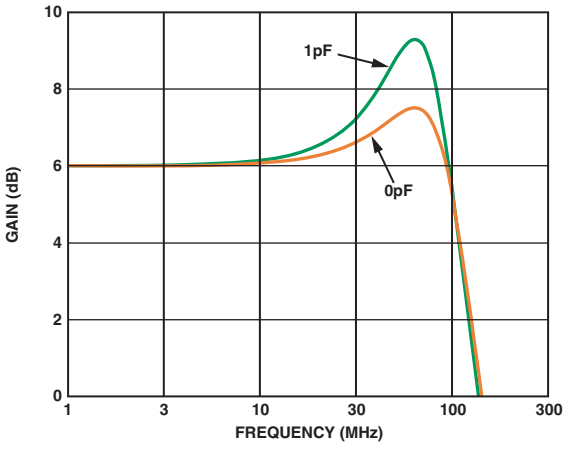

Figure 4. Additional peaking caused by parasitic capacitance.

A few basic formulas for calculating the size of those gremlins can come in handy when seeking the sources of the problematic parasitics. Equation 1 is the formula for a parallel-plate capacitor (see Figure 5).

$$C = \frac{kA}{11.3d}\,\text{pF} \tag{1}$$

C is the capacitance, A is the area of the plate in cm^2, k is the relative dielectric constant of board material, and d is the distance between the plates in centimeters.

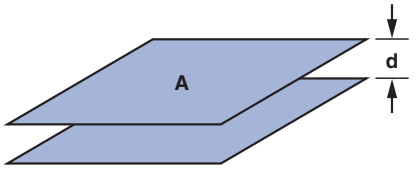

Figure 5. Capacitance between two plates.

Strip inductance is another parasitic to be considered, resulting from excessive trace length and lack of ground plane. Equation 2 shows the formula for trace inductance. See Figure 6.

$$\text{Inductance} = 0.0002L\left[\ln\frac{2L}{(W+H)} + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu\text{H} \tag{2}$$

W is the trace width, L is the trace length, and H is the thickness of the trace. All dimensions are in millimeters.

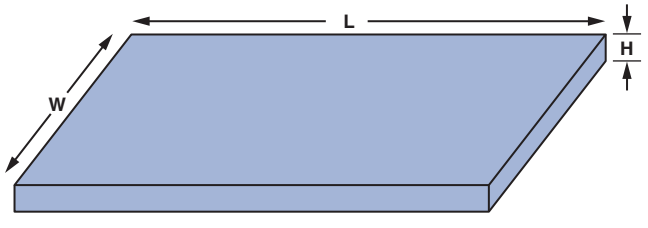

Figure 6. Inductance of a trace length.

The oscillation in Figure 7 shows the effect of a 2.54-cm trace length at the noninverting input of a high-speed op amp. The equivalent stray inductance is 29 nH (nanohenry), enough to cause a sustained low-level oscillation that persists throughout the period of the transient response. The picture also shows how using a ground plane mitigates the effects of stray inductance.

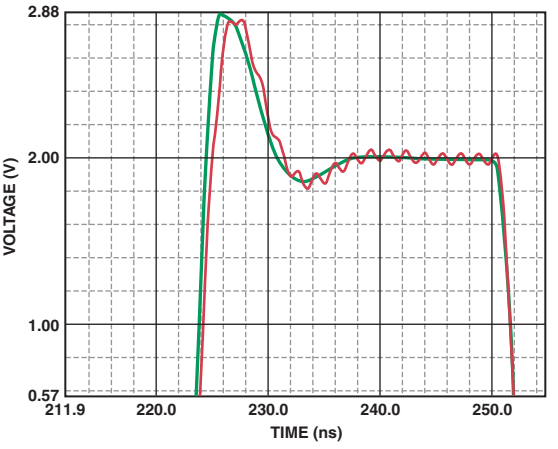

Figure 7. Pulse response with—and without—ground plane.

Vias are another source of parasitics; they can introduce both inductance and capacitance. Equation 3 is the formula for parasitic inductance (see Figure 8).

$$L = 2T\left[\ln\frac{4T}{d} + 1\right]\text{nH} \tag{3}$$

T is the thickness of the board and d is the diameter of the via in centimeters.

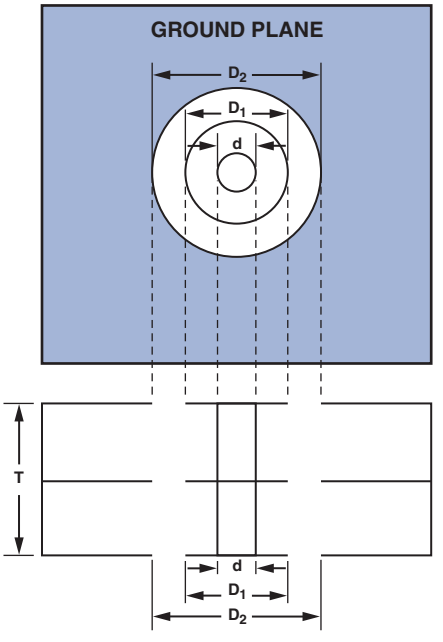

Figure 8. Via dimensions.

Equation 4 shows how to calculate the parasitic capacitance of a via (see Figure 8).

$$C = \frac{0.55\varepsilon_r TD_1}{D_2 - D_1}\,\text{pF} \tag{4}$$

ε_r is the relative permeability of the board material. T is the thickness of the board. D_1 is the diameter of the pad surrounding the via. D_2 is the diameter of the clearance hole in the ground plane. All dimensions are in centimeters. A single via in a 0.157-cm-thick board can add 1.2 nH of inductance and 0.5 pF of capacitance; this is why, when laying out boards, a constant vigil must be kept to minimize the infiltration of parasites!

Ground Plane

There is much more to discuss than can be covered here, but we'll highlight some of the key features and encourage the reader to pursue the subject in greater detail. A list of references appears at the end of this article.

A ground plane acts as a common reference voltage, provides shielding, enables heat dissipation, and reduces stray inductance (but it also increases parasitic capacitance). While there are many advantages to using a ground plane, care must be taken when implementing it, because there are limitations to what it can and cannot do.

Ideally, one layer of the PCB should be dedicated to serve as the ground plane. Best results will occur when the entire plane is unbroken. Resist the temptation to remove areas of the ground plane for routing other signals on this dedicated layer. The ground plane reduces trace inductance by magnetic-field cancellation between the conductor and the ground plane. When areas of the ground plane are removed, unexpected parasitic inductance can be introduced into the traces above or below the ground plane.

Because ground planes typically have large surface and cross-sectional areas, the resistance in the ground plane is kept to a minimum. At low frequencies, current will take the path of least resistance, but at high frequencies current follows the path of least *impedance*.

Nevertheless, there are exceptions, and sometimes less ground plane is better. High-speed *op amps* will perform better if the ground plane is removed from under the input and output pads. The stray capacitance introduced by the ground plane at the input, added to the op amp's input capacitance, lowers the phase margin and can cause instability. As seen in the parasitics discussion, 1 pF of capacitance at an op amp's input can cause significant peaking. Capacitive loading at the output—including strays—creates a pole in the feedback loop. This can reduce phase margin and could cause the circuit to become unstable.

Analog and digital circuitry, including grounds and ground planes, should be kept separate when possible. Fast-rising edges create current spikes flowing in the ground plane. These fast current spikes create noise that can corrupt analog performance. Analog and digital grounds (and supplies) should be tied at one common ground point to minimize circulating digital and analog ground currents and noise.

At high frequencies, a phenomenon called *skin effect* must be considered. Skin effect causes currents to flow in the outer surfaces of a conductor—in effect making the conductor narrower, thus increasing the resistance from its dc value. While skin effect is beyond the scope of this article, a good approximation for the skin depth in copper, in centimeters, is

$$\text{Skin Depth} = \frac{6.61}{\sqrt{f(\text{Hz})}} \qquad (5)$$

Less susceptible plating metals can be helpful in reducing skin effect.

Packaging

Op amps are typically offered in a variety of packages. The package chosen can affect an amplifier's high-frequency performance. The main influences are parasitics (mentioned earlier) and *signal routing*. Here we will focus on routing inputs, outputs, and power to the amplifier.

Figure 9 illustrates the layout differences between an op amp in an SOIC package (a) and one in an SOT-23 package (b). Each package type presents its own set of challenges. Focusing on (a), close examination of the feedback path suggests that there are multiple options for routing the feedback. Keeping trace lengths short is paramount. Parasitic inductance in the feedback can cause ringing and overshoot. In Figures 9(a) and 9(b), the feedback path is routed around the amplifier. Figure 9(c) shows an alternative approach—routing the feedback path under the SOIC package—which minimizes the feedback path length. Each option has subtle differences. The first option can lead to excess trace length, with increased series inductance. The second option uses vias, which can introduce parasitic capacitance and inductance. The influence and implications of these parasitics must be taken into consideration when laying out the board. The SOT-23 layout is almost ideal: minimal feedback trace length and use of vias; the load and bypass capacitors are returned with short paths to the same ground connection; and the positive rail capacitors, not shown in Figure 9(b), are located directly under the negative rail capacitors on the bottom of the board.

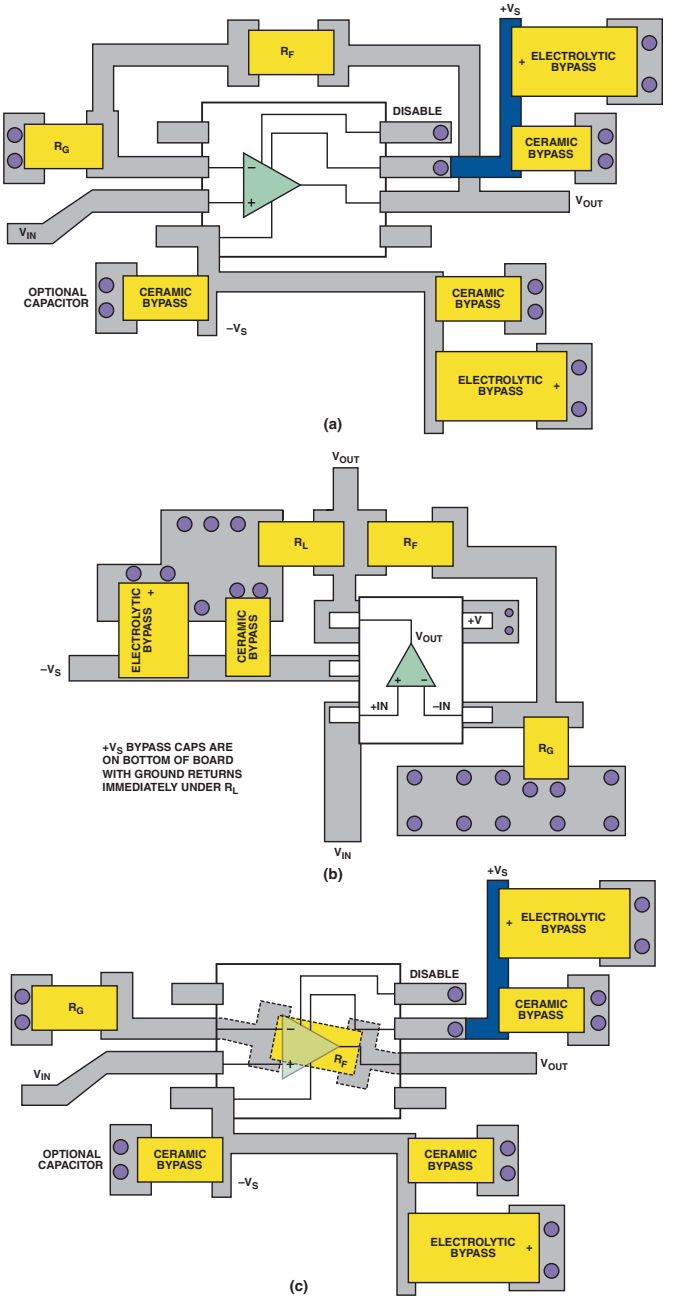

Figure 9. Layout differences for an op amp circuit. (a) SOIC package, (b) SOT-23, and (c) SOIC with R_F underneath board.

Low-distortion amplifier pinout: A new low-distortion pinout, available in some Analog Devices op amps (the AD8045,[1] for example), helps eliminate both of the previously mentioned problems; and it improves performance in two other important areas as well. The LFCSP's low-distortion pinout, as shown in Figure 10, takes the traditional op amp pinout, rotates it counterclockwise by one pin and adds a second output pin that serves as a dedicated feedback pin.

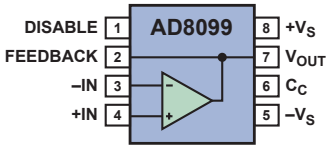

Figure 10. Op amp with low-distortion pinout.

The low-distortion pinout permits a close connection between the output (the dedicated feedback pin) and the inverting input, as shown in Figure 11. This greatly simplifies and streamlines the layout.

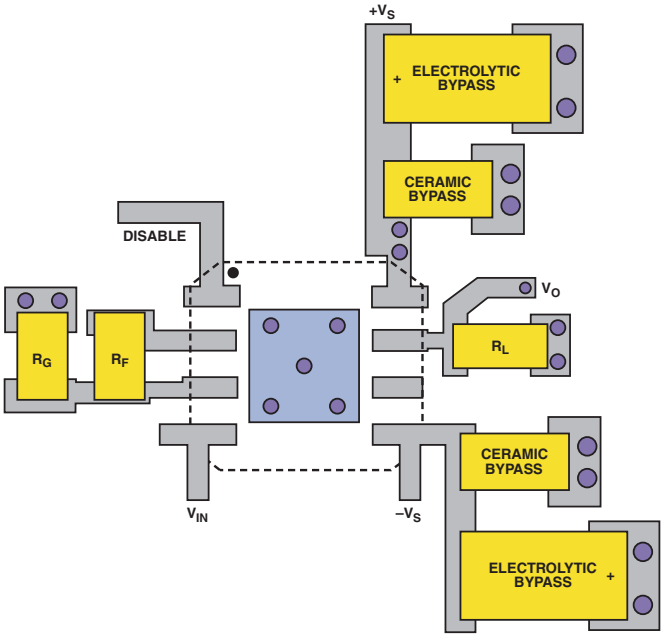

Figure 11. PCB layout for AD8045 low-distortion op amp.

Another benefit is decreased second-harmonic distortion. One cause of second-harmonic distortion in conventional op amp pin configurations is the coupling between the noninverting input and the negative supply pin. The low-distortion pinout for the LFCSP package eliminates this coupling and greatly reduces second-harmonic distortion; in some cases the reduction can be as much as 14 dB. Figure 12 shows the difference in distortion performance between the AD8099[2] SOIC and the LFCSP package.

This package has yet another advantage—in power dissipation. The LFCSP provides an exposed paddle, which lowers the thermal resistance of the package and can improve θ_{JA} by approximately 40%. With its lower thermal resistance, the device runs cooler, which translates into higher reliability.

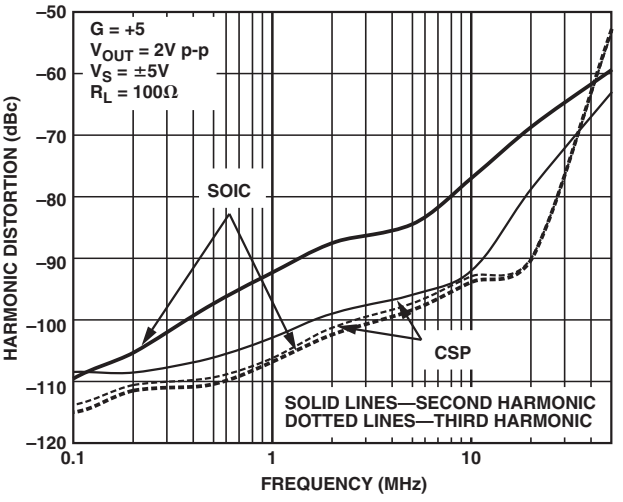

Figure 12. AD8099 distortion comparison—the same op amp in SOIC and LFCSP packages.

At present, three Analog Devices high-speed op amps are available with the new low-distortion pinout: AD8045, AD8099, and AD8000.[3]

Routing and Shielding

A wide variety of analog and digital signals, with high- and low voltages and currents, ranging from dc to GHz, exists on circuit boards. Keeping signals from interfering with one another can be difficult.

Recalling the advice to "trust no one," it is critical to think ahead and come up with a plan for how the signals will be processed on the board. It is important to note which signals are sensitive and to determine what steps must be taken to maintain their integrity. Ground planes provide a common reference point for electrical signals, and they can also be used for shielding. When signal isolation is required, the first step should be to provide physical distance between the signal traces. Here are some good practices to observe:

- Minimizing long parallel runs and close proximity of signal traces on the same board will reduce inductive coupling.
- Minimizing long traces on adjacent layers will prevent capacitive coupling.
- Signal traces requiring high isolation should be routed on separate layers and—if they cannot be totally distanced—should run orthogonally to one another with ground plane in between. Orthogonal routing will minimize capacitive coupling, and the ground will form an electrical shield. This technique is exploited in the formation of *controlled-impedance* lines.

High-frequency (RF) signals are typically run on controlled-impedance lines. That is, the trace maintains a characteristic impedance, such as 50 Ω (typical in RF applications). Two common types of controlled-impedance lines, *microstrip*[4] and *stripline*[5] can both yield similar results, but with different implementations.

A microstrip controlled-impedance line, shown in Figure 13, can be run on either side of a board; it uses the ground plane immediately beneath it as a reference plane.

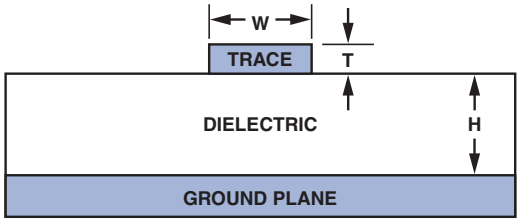

Figure 13. A *microstrip* transmission line.

Equation 6 can be used to calculate the characteristic impedance for an FR4 board.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r} + 1.41} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \quad (6)$$

H is the distance in from the ground plane to the signal trace, W is the trace width, T is the trace thickness; all dimensions are in mils (inches $\times 10^{-3}$). ε_r is the dielectric constant of the PCB material.

Stripline controlled-impedance lines (see Figure 14) use two layers of ground plane, with signal trace sandwiched between them. This approach uses more traces, requires more board layers, is sensitive to dielectric thickness variations, and costs more—so it is typically used only in demanding applications.

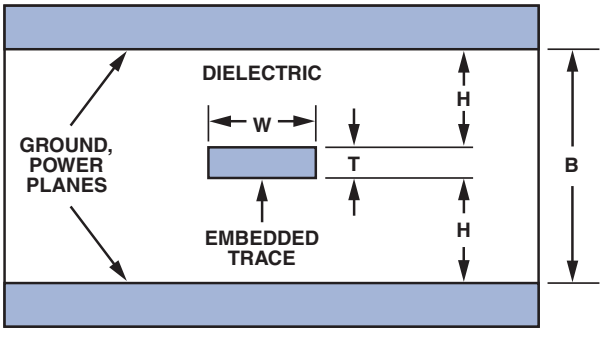

Figure 14. Stripline controlled-impedance line.

The characteristic-impedance design equation for stripline is shown in Equation 7.

$$Z_0(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right] \quad (7)$$

Guard rings, or "guarding," is another common type of shielding used with op amps; it is used to prevent stray currents from entering sensitive nodes. The principle is straightforward—completely surround the sensitive node with a guard conductor that is kept at, or driven to (at low impedance) the same potential as the sensitive node, and thus sinks stray currents away from the sensitive node. Figure 15(a) shows the guard ring schematics for inverting and noninverting op amp configurations. Figure 15(b) shows a typical implementation of both guard rings for a SOT-23-5 package.

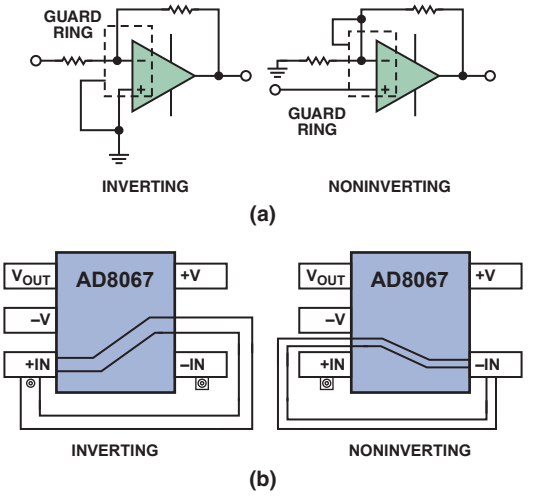

Figure 15. Guard rings. (a) Inverting and noninverting operation. (b) SOT-23-5 package.

There are many other options for shielding and routing. The reader is encouraged to review the references below for more information on this and other topics mentioned above.

CONCLUSION

Intelligent circuit-board layout is important to successful op amp circuit design, especially for high-speed circuits. A good schematic is the foundation for a good layout; and close coordination between the circuit designer and the layout designer is essential, especially in regard to the location of parts and wiring. Topics to consider include power-supply bypassing, minimizing parasitics, use of ground planes, the effects of op amp packaging, and methods of routing and shielding.

FOR FURTHER READING

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3 ADI website: www.analog.com (Search) AD8000 (Go)
4 http://www.microwaves101.com/encyclopedia/microstrip.cfm
5 http://www.microwaves101.com/encyclopedia/stripline.cfm

This article can be found at http://www.analog.com/library/analogdialogue/archives/39-09/layout.html, with a link to a PDF.

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Filter, Video, triple, with selectable cutoff frequencies, RGB, HD, SD **ADA4412-3**
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Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 39 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

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ANALOG DEVICES

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Direct Digital Synthesis (DDS) Controls Waveforms in Test, Measurement, and Communications

By Eva Murphy [eva.murphy@analog.com]
Colm Slattery [colm.slattery@analog.com]

In many kinds of equipment, it is important to produce and readily control accurate waveforms of various frequencies and profiles. Examples include agile frequency sources with low phase noise and low spurious signal content for communications, and simply generated frequency stimuli for industrial and biomedical applications. In such applications, the ability to generate an adjustable waveform conveniently and cost effectively is a key design consideration.

Various approaches have been used, but the most flexible one is *direct digital synthesis*[1] (DDS). A DDS chip[2], or *direct digital synthesizer*, produces an analog waveform—usually a sine wave, but triangular and square waves are inherent—by generating a time-varying signal in digital form and then performing a digital-to-analog (D/A) conversion. DDS devices are primarily digital, so they can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies.

With advances in design and process technology, today's DDS devices are very compact and draw little power. Currently available DDS devices[3] can generate frequencies from well below 1 Hz up to 400 MHz (based on a 1-GHz clock), with time resolution to 48 bits. The low cost of devices using new process technologies—combined with DDS's inherently excellent performance and the ability to digitally (re)program the output waveform—make the DDS approach extremely attractive compared to more discrete and less flexible traditional solutions. Multichannel DDS devices, such as the 2-channel AD9958[4] and the 4-channel AD9959,[5] allow independent programming of up to four inherently synchronized outputs in space-constrained systems (e.g., phased-array radar/sonar, ATE, medical imaging, and optical communications).

Our objective here is to provide the reader with an understanding of a few important uses of DDS in existing applications, and to provide an insight into the key benefits the DDS device brings to these—and other potential applications. At present, the two principal forms of applications using DDS are waveform generation in *communications*—and signal analysis in *industry* and *biomedicine*. Typical other uses include electronic article surveillance (EAS) and maritime applications in sonobuoy systems.

Important applications exist in communications systems that require agile frequency sources with low phase noise and spurs, combining—as DDS does—excellent frequency-tuning resolution and spectral performance. Other typical DDS uses in communications include generating pilot signals for WDM optical-channel identification, enhanced-tunability reference frequencies for phase-locked loops (PLLs), as local oscillators, or even for direct transmission.

In the signal analysis category, many industrial and biomedical designs use DDS to digitally generate programmable waveforms with easily adjustable frequency and phase—without the need to change any external components, as is often the case with traditional waveform generators. Simple frequency adjustments can be used to locate resonances or compensate for temperature drifts. A DDS can be used as a flexible frequency stimulus in measuring sensor impedance, or to generate pulse-width-modulated signals for microactuators, or to examine attenuation in LANs or telephone cables.

Applications in Industry and Medicine

Signal-generator network analysis: Many applications in electronics today involve gathering and decoding data for digital signal processing, analog measurements, fiber optics, and high-frequency communications.

This class of application involves stimulating a circuit or system with frequencies of known amplitude and phase, and analyzing the characteristics of the response to provide key system information. The *network under analysis* (Figure 1) can be anything from a length of cable to a measurement/sensor system. The typical requirement is to compare the response signal(s) to the input signal in phase, frequency, and amplitude.

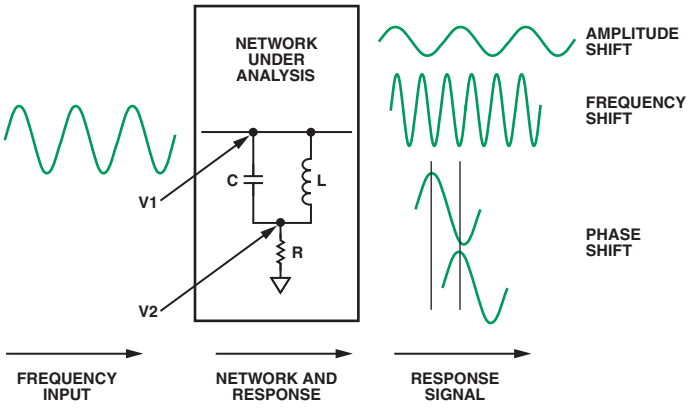

Figure 1. Response testing.

Where a train of frequencies is needed for excitation, a DDS chip is just right, since the stimulus frequency, phase, and amplitude can be software controlled with very tight resolution.

The system works by applying a signal having known frequency, amplitude, and phase to point V1 of the network (shown as a passive circuit for the sake of simplicity) in Figure 2. The amplitude and phase of the signal at point V2 will vary depending on the characteristics of the network. The time difference between the signals, V2 and V1, allows the user to calculate the phase shift, and the change in magnitude will give the relative amplitude shift. Differences in their frequency spectra can provide a measure of distortion. Knowing both the phase- and amplitude response of the system under test, it is possible to calculate its transfer function.

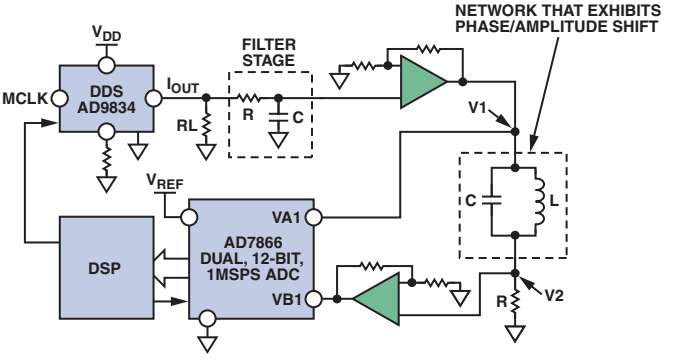

Figure 2. System block diagram.

Typical frequencies used in these applications tend to be from 0 kHz to 200 kHz, at the low end of the DDS frequency-handling range. For some applications a burst of one known frequency provides sufficient information; but for most it is required to sweep a range of known frequencies across the network and analyze the phase/amplitude data for multiple frequencies. A single DDS chip provides the entire frequency generation function, giving the user great flexibility in digitally controlling the frequencies required

for network control. With no external components required, the user just needs the ability to write to the DDS through its SPI interface. The output phase of the DDS is typically controllable with 10-bit-to-14-bit resolution, giving programmable phase resolution to <0.1 degrees.

In the system of Figure 2, the AD9834 DDS chip is used as the analog stimulus for the system. It is driven with a 50-MHz crystal oscillator. The frequency resolution of the AD9834 is 28 bits, which allows the frequency to be controlled to about 0.2 Hz. The DDS output amplitude is controlled by an external resistance to ground; and an external gain stage drives the network.

The output, loaded by resistor, RL, drives a low-pass RC filter, which band-limits the signal and filters out clock frequency, images, and higher frequencies. A buffer amplifier drives the network, represented here by an LRC circuit. The reference signal is connected to Channel 1 of a 2-channel, simultaneous-sampling ADC (such as the AD7866[6] 12-bit, 1-MSPS, dual ADC); and the response signal is applied to Channel 2 of the ADC.

A digital signal processor, used as a system controller, controls the DDS and the ADC sampling. The DSP handles the processing requirements of the system with simple arithmetic, or by FFT, DFT, or proprietary algorithms, and may also control any necessary amplitude- and phase calibration of the system.

Other Applications

A similar approach may be used in many other applications, with variations that depend on the physics and circuitry employed. Examples include providing frequency sweeps for use in testing LVDTs (linear variable differential transformers); proximity sensing using a capacitive sensor; metal detection using balanced coils; blood measurement using a chemical sensor; flow measurement using ultrasonic sensors; and electronic article surveillance (EAS)—to prevent shoplifting—using RF-responding tags.

DDS in Communications

Classically, when considering the design of a new frequency synthesizer, two basic approaches have been common: *phase-locked loops* (PLL) and *direct digital synthesis*. The choice is not always clear-cut; often the designer must make trade-offs or design additional circuitry to compensate for the weaknesses of the chosen technique.

However, now that both PLL and DDS circuits are available as low-cost components, it is becoming practical to consider designing a hybrid circuit combining both techniques, thus eliminating the trade-offs. The designer can take advantage of both methods to obtain an overall solution that outperforms individual PLL or DDS designs. We will discuss approaches with the benefits of:

- fine frequency resolution
- fast switching action
- fast settling time
- wide bandwidth
- very low power
- low phase noise and spurious noise

Two different PLL/DDS hybrid frequency synthesizers will be discussed here—a DDS providing a fine-tunable reference for a PLL, and a PLL with the internal offset from the local-oscillator (LO) frequency generated by a DDS.

Fine-tunable reference for a PLL: Figure 3 shows a phase-locked-loop frequency synthesizer with the reference frequency generated by the filtered output of a DDS. By using a hybrid solution, the tuning resolution of the DDS can enhance the tunability of the overall system to a level not possible with a PLL alone.

In this example, the PLL consists of an integer-N ADF4106[7] frequency synthesizer, plus an external loop filter and VCO. This configuration allows the designer to choose a VCO to meet the frequency conditions and a loop filter to fit the needs of the application. The reference is generated by an AD9834[8] DDS, followed by a filter and optional matched divider, for reducing noise and spurs.

The DDS, with its 28-bit tuning word, allows the reference frequency to be very narrowly tuned, resulting in fine adjustment of the output frequency much more conveniently than through the use of a fractional-N PLL.

For example, if the VCO has a frequency range of 100 MHz to 500 MHz, and the DDS output is in the neighborhood of 5 MHz, the range of N is from 20 to 100. Each step of N results in a 5-MHz step of output frequency (100 MHz, 105 MHz, 110 MHz, etc.) However, the AD9834's output can be set in small increments by simply adjusting the hexadecimal number written to the frequency register. The AD9834 can be tuned in increments as small as 0.2 Hz with a 50-MHz clock rate. This results in very fine tuning of the hybrid PLL/DDS.

Ideally, the reference would have low phase noise and spurious tones. The DDS output does indeed have low phase noise, but its spurious content may need to be addressed at some frequencies. The spurs are due to a truncation after the phase accumulator, which results in increased spurious content at particular sampling/output frequency combinations. These spurs may be minimized with additional filtering and a careful choice of sampling plan.

If switching speed is unimportant, the PLL bandwidth can be made extremely narrow to exclude reference spurs; then the phase noise and spurs are limited to those of the VCO. If the VCO is clean, this may be the simplest way to obtain a synthesizer with a wide bandwidth, fine resolution, good spurious noise, small size, and extremely low power, albeit with slow switching between frequencies.

To take advantage of the DDS's fast switching ability, as well as its high resolution, a wider PLL loop-bandwidth is needed—making the filter and the optional divider important for low noise and spurs. Note that the PLL increases the amplitude of the spurious tones, but not their frequency offset from the reference. Thus the filter in Figure 3 is necessary to confine the DDS-generated spurious tones and noise to a narrow bandwidth. After frequency multiplication by N, the noise and spurious tones will be increased by 20 log(N), but only within the filter bandwidth. Ultimately, the selection of

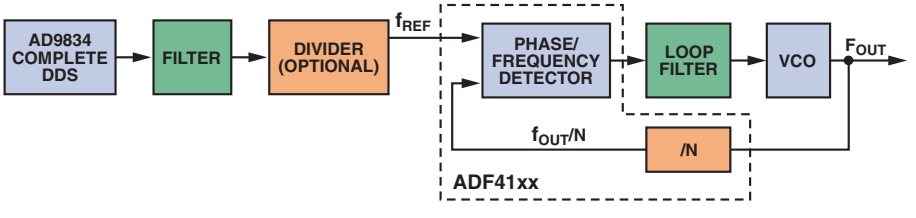

Figure 3. DDS as reference-frequency generator for a PLL.

the filter bandwidth and center frequency is a trade-off between switching speed, noise performance, and the need for continuous frequency coverage.

PLL with the internal offset frequency generated by a DDS: Figure 4 shows a phase-locked-loop synthesizer with the internal offset frequency generated by a DDS.

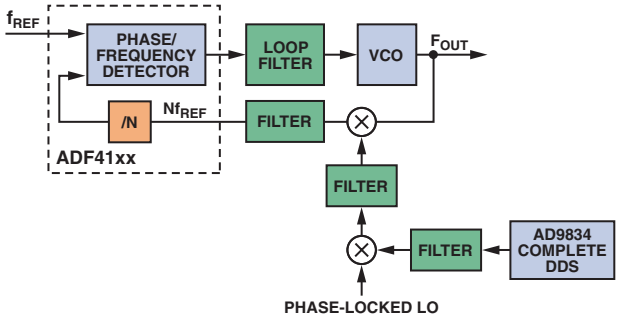

Figure 4. The AD9834 DDS generates the frequency offset for the ADF41xx PLL.

This circuit uses a finely set DDS frequency to modulate a local oscillator frequency, producing a sum/difference frequency which, when filtered, modulates the reference frequency, producing an output frequency,

$$f_{OUT} = Nf_{REF} \pm \left(f_{LO} \pm f_{OFFSET}\right)$$

This is similar to multiloop synthesizer design, except that the fine-frequency-step PLLs are replaced by a single DDS. The fine frequency resolution of the DDS in this hybrid synthesizer can provide better frequency resolution than a PLL with many loops.

The PLL provides the coarse steps and, as before, the PLL output frequency (with the local oscillator) has the same basic resolution as the input reference frequency, f_{REF}. The DDS provides fine steps between each of the coarse steps, so that the ultimate output step size is that of the DDS. Using an AD9834 with a 50-MHz master clock, a step size of 0.2 Hz is possible.

DDS in Data Encoding

Because DDS devices make adjustment of frequency and phase an easy matter, they are especially useful in encoding data for phase- and frequency modulation onto a carrier. Here are two related applications harking back to the early days of radiotelegraphy.

FSK encoding: Binary *frequency-shift keying* (FSK) is one of the simplest forms of data encoding. The data is transmitted by shifting the frequency of a continuous carrier to one or the other of two discrete frequencies (a binary operation). One frequency (f_1) is designated as the "mark" frequency (binary *one*) and the other (f_0) as the "space" frequency (binary *zero*). Figure 5 shows the relationship between the data and the transmitted signal.

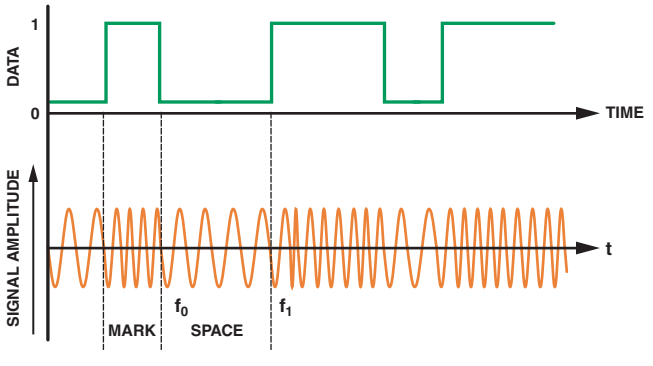

Figure 5. FSK modulation.

This encoding scheme is easily implemented using a DDS. The DDS frequency tuning word representing the output frequencies changes in order to generate f_0 and f_1 in synchronism with the pattern of 1s and 0s to be transmitted. The user programs the tuning words corresponding to the chosen frequencies into the device before transmission. In the case of the AD9834, two frequency registers are conveniently available for FSK encoding. A dedicated pin on the device (FSELECT) is used to select the frequency register corresponding to the appropriate tuning word. The block diagram in Figure 6 demonstrates the implementation of FSK encoding.

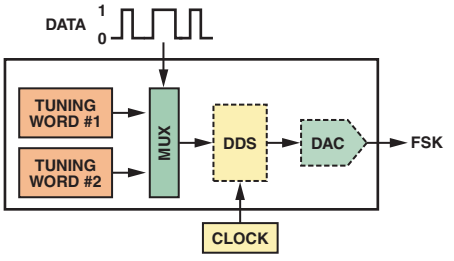

Figure 6. A DDS-based FSK encoder.

PSK encoding: *Phase-shift keying* (PSK) is another simple form of data encoding. In PSK, while the frequency of the carrier remains constant, the phase of the transmitted signal is varied to convey the information.

There are various schemes that can be used to accomplish PSK. The simplest method, using only two signal phases—0° and 180°—is commonly known as *binary PSK* (BPSK). 0° corresponds to Logic 1, and 180° corresponds to Logic 0. The state of each bit received is determined according to the state of the preceding bit. If the phase of the wave does not change, the signal state stays the same (low or high). If the phase of the wave reverses, i.e., changes by 180°, the signal state changes (from low to high, or from high to low).

PSK encoding is easily implemented with DDS products. Most of the devices have a separate input register (a *phase register*) that can be loaded with a phase value. This value is directly added to the phase of the carrier without changing its frequency. Changing the contents of this register modulates the phase of the carrier (thus generating a PSK output signal). For applications that require high-speed modulation, the AD9834 allows the preloaded phase registers to be selected using a dedicated input pin (PSELECT); toggling this pin modulates the carrier as required.

Other phase angles may be used. More complex forms of PSK employ four or eight different phases. This allows binary data to be transmitted at a faster rate per phase change than is possible with BPSK modulation. For example, in four-phase modulation, *quadrature PSK* (QPSK), the possible phase angles are 0°, +90°, –90°, and 180°; each phase shift can represent two data bits. The AD9830,[9] AD9831,[10] AD9832,[11] and AD9835[12] provide four phase registers to allow complex phase-modulation schemes to be implemented by continuously updating different phase offsets to the registers.

Sonobuoy applications: DDS is useful in *sonobuoy* communications. A sonobuoy is a device that lies in the water and captures ambient sounds in the ocean. Common applications for sonobuoys are in the detection, localization, identification, and tracking of seismic events and underwater targets such as submarines and whales. Arrays of sonobuoys can be used to determine target position, velocity, and direction.

There are four main components to a sonobuoy: a float, a radio transceiver, a battery, and a hydrophone. The hydrophone is an underwater sensor that converts sound pressure waves into electrical voltages that get amplified and sent up to the surface

float. The radio signal is picked up by an antenna and a radio receiver, usually on an aircraft or a ship.

Active sonobuoys transmit sound waves, which bounce off objects. The distance and direction to the object can be determined from the reflected signal. A transducer is used to introduce the acoustic wave into the water and to manipulate the return echoes, which are then amplified for VHF radio transmission. Passive sonobuoys do not emit any sound; they just sit and listen for incoming sounds. In both cases the data is transmitted back to a ship or aircraft, often using spread-spectrum communications, in which the frequencies are rapidly hopped about so as to resemble random noise. A DDS is often used to provide the frequency hopping in the *transmit* and *receive* sections.

The AD9834 is ideal as an agile frequency source in the transmitter section of the sonobuoy (Figure 7). Typical frequencies transmitted are from 136 MHz to 174 MHz.

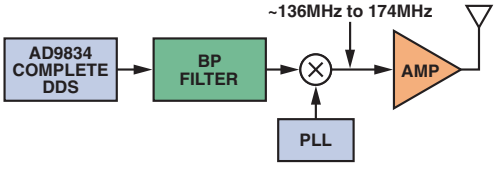

Figure 7. DDS in *transmit* section of sonobuoy.

A block diagram of a typical receiver, for GPS position location, is shown in Figure 8.

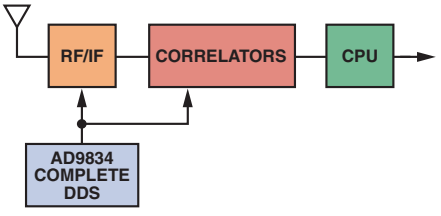

Figure 8. DDS in *receive* section of sonobuoy.

The receive portion of the sonobuoy consists of a GPS antenna, low-noise amplifier, and downconversion front-end stage. The downconversion is driven by the DDS. The signal from the front end is sampled and digitized, and the resulting data stream (which contains the spread-spectrum data of all GPS satellites in range of the antenna) is passed to correlators for spread-spectrum processing. The output of the correlation process is converted by the CPU to provide the sonobuoy's coordinates.

The DDS offers advantages for both the transmitter and receiver, because of its fine-tuning capabilities. The low power (25 mW) and low cost of the AD9833/AD9834 make them an ideal solution for battery-powered, disposable applications, such as in sonobuoys.

Fiber optic channel identification: Communication using light waves over fiber optic cables has greatly increased bandwidth and capacity over that available with copper-core technology. Capacity is increased further by using the multiple channels that *wavelength division multiplexing* (WDM) can make available at relatively low cost.

WDM involves combining separate light wavelengths (colors) from the various simultaneous input data streams, and transmitting the sum of these channels ("white" light) through a single optical fiber. Different protocols can be mixed within the same link. At the receiving end, the light is separated into its components, and demodulated.

Although all of the signals are transmitted at the same time, it is desirable to identify from which channel a signal originated. One way to distinguish between channels is to add a pilot signal with identifiable parameters (e.g., amplitude, frequency, phase, etc.) to each channel's digital data. In optical transmitters the pilot signal is added by varying the current flowing through the laser diode. Figure 9 shows how this is done.

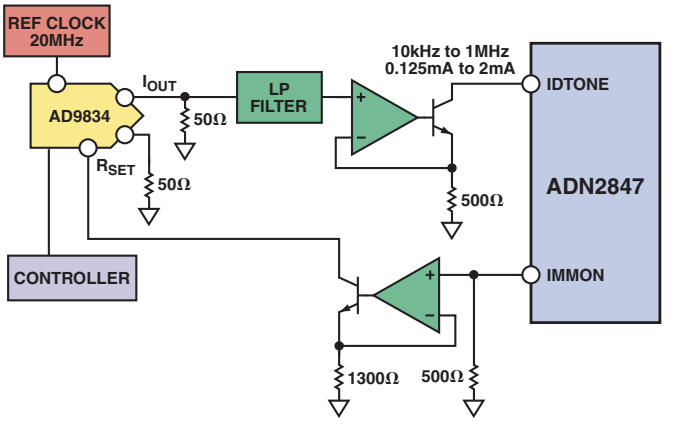

Figure 9. DDS in an optical-fiber communications application.

The ADN2847 laser-diode driver operates at any rate between 50 Mbps and 3.3 Gbps. An external sink current at IDTONE, supplied for fiber identification in WDM, modulates the *optical 1* level over a possible range of 2% of minimum Imod to 10% of maximum Imod. The AD9834 generates the modulation waveform and controls the current sinking out of IDTONE by controlling the voltage across a 500 Ω resistor. A dc current on IMMON, reflecting the modulation current, is used in a feedback loop to control the AD9834 output level via its R_{SET} pin.

CONCLUSION

Direct digital synthesis, which generates analog waveforms with digitally adjustable high-resolution phase and frequency, is useful in a wide variety of applications in test, measurement, and communications. Integrated-circuit DDS devices are compact, require little power and space, are low in cost, and easy to apply.

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This article can be found at http://www.analog.com/library/analogdialogue/archives/39-08/dds_apps.html, with a link to a PDF.

Encoder's Spare Channel Embeds Whole-House Stereo Audio in Satellite Set-Top-Box Designs Stably and Cost-Effectively

By Jeritt Kent [jeritt.kent@analog.com] and Victor Chang

INTRODUCTION

Satellite set-top boxes (STBs) and television receivers contain a number of chips that require high-speed clocks. If the video decoder chip does not have an external clock drive—and many newer devices do not—a clock must be indirectly generated for any audio components that require it. This article shows how a *phase-locked loop* (PLL) can be used to derive a stable high-speed clock for a *Broadcast-Television-Systems-Committee* (BTSC) stereo-enabled system, employing a dual-channel BTSC encoder, such as the AD71028.[1]

One channel of the encoder handles the actual BTSC stereo-encoded output, and the second channel serves to derive both the primary channel's master clock and its own subsidiary clock—using the vestigial pilot signal in the BTSC composite audio spectrum plus negative-feedback error correction. With the AD71028 used in this way, stereo capability can be added inexpensively when designing a satellite STB. For the consumer, this means that in homes where TVs and *audio/video* (A/V) receivers are in multiple rooms, BTSC stereo can be fed throughout the house via coaxial cables, avoiding the high cost and low noise immunity of RCA audio/video cables.

This article describes the clock-generation problem in the set-top-box environment—and then shows a compact, low-cost solution that both generates a stable system master clock and derives a clock for the stereo audio distribution system.

Multichannel television sound (MTS), better known as BTSC encoding—developed by Zenith—was adopted by the U.S. *Federal Communications Commission* (FCC) in 1984 as the method for encoding three additional audio channels onto *National Television Systems Committee* (NTSC) format video signals. Early NTSC video already included a monophonic audio signal (equivalent to L + R, stereo-sum), so BTSC added the stereo difference signal (L – R), which is combined with the sum signal to decode stereo audio. In addition, a second channel, known as *second audio program* (SAP), is available to provide a second language, an audio description service for the visually impaired, or radio service. A third—*professional* (PRO)—channel may be used by the broadcasting station for audio or data exchange.

Frequency plots of NTSC composite video and BTSC composite audio spectra are shown in Figures 1 and 2, respectively. Note that the BTSC spectrum incorporates a pilot signal at 15.734 kHz, which is the same frequency as the NTSC video horizontal sync, 1H = f_{Hsync}. This pilot signal is used by the receiver to recover the *double-sideband suppressed-carrier* (DSBSC) modulated stereo-difference (L – R) audio channel at 2H, and the SAP and PRO channels at 5H and 6.5H. It is important to note that DSBSC modulation requires *coherent* demodulation, so phase and frequency must be identical at both transmit and receive points to avoid severe distortion.

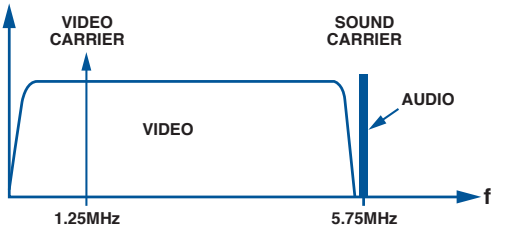

Figure 1. NTSC spectrum for a television channel.

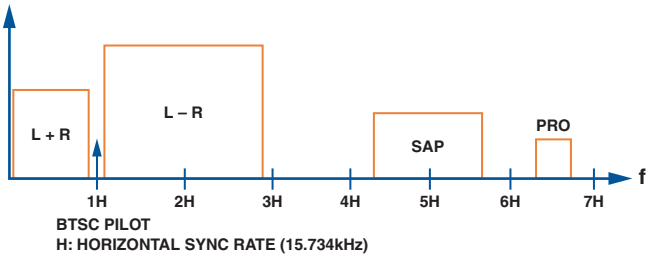

Figure 2. Audio spectrum defined by BTSC.

In receiver designs, a *phase-locked loop* (PLL) is used in the *local oscillator* (LO) to eliminate frequency- and phase offsets due to environmental effects—such as ambient temperature changes. Since these offsets cause errors in downconversion and demodulation, standalone oscillators are inadequate because they track neither frequency nor phase. A typical PLL contains a low-drift reference oscillator and a *voltage-controlled oscillator* (VCO) that provides frequency tuning. Using negative feedback, a low drift output is generated from the reference input. Because f_{Hsync} can be used as a low-drift reference signal, a PLL can be used to generate the master clock for the BTSC encoder and *analog-to-digital converter* (ADC). The traditional method uses a PLL to produce a master clock, but the circuit presented here uses an unusual technique: it incorporates a device that *requires* a master clock into the PLL feedback loop that *generates* the master clock.

In its most basic form, the PLL consists of a phase detector, loop filter, and VCO, as shown in Figure 3. The phase detector compares the phase of the reference signal to the feedback signal, and produces a slowly varying output as a function of the difference. The phase detector's output is filtered to provide a clean control voltage for the VCO. The VCO output is fed back to the phase detector, and the negative feedback forces the VCO to generate a frequency equal to the reference frequency at equilibrium. Shifts in the frequency or phase (rate-of-change of frequency) of the reference signal will be tracked by the phase detector. The filtered output of the phase detector drives the VCO, causing it to follow the reference frequency. When the VCO output frequency and phase are equal to the reference signal, the PLL is said to be in a "locked" condition.

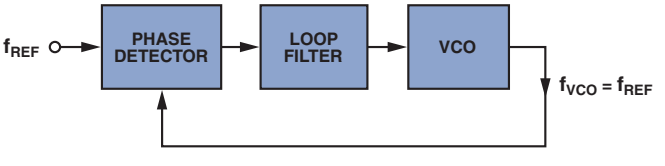

Figure 3. Basic PLL system.

With slight modifications, this basic PLL principle can be applied in many useful ways. For instance, by adding a frequency divider in the loop (for example, a modulo-N counter), as shown in Figure 4, the basic PLL becomes a stable and tunable frequency synthesizer, which generates a VCO output frequency that may be an integer- or fractional multiple of the input reference frequency, $f_{VCO} = N \times f_{REF}$.

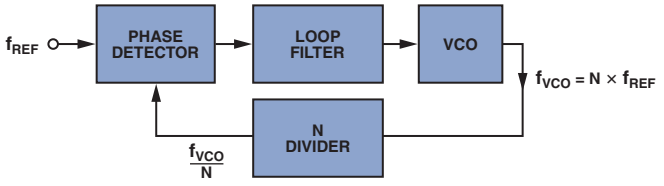

Figure 4. PLL frequency synthesizer. When the loop settles, $f_{VCO} = N \times f_{REF}$.

STBs and television receivers contain multiple chips that require high-speed clocks. *Moving-Picture-Experts-Group* (MPEG) based receivers, for example, use a 27-MHz master clock that must be routed to the supplemental audio components. The source of this clock is often the MPEG decoder chip, but if the MPEG decoder does not provide it externally, it must be generated elsewhere. The following application in a BTSC-enabled system employs PLL principles to use an AD71028 dual-channel BTSC encoder as the fractional divider that derives a stable, high-speed, frequency- and phase-locked clock. One channel of the encoder is used for the BTSC stereo-encoded output, while the second channel is used with negative feedback to derive the master clock for both the primary channel and for the encoder itself.

In this application, the AD71028 inexpensively adds stereo capability to satellite STBs without the need for a 27-MHz clock source. In homes where TVs and *audio/video receivers* (AVRs) are used in various rooms, this technique allows the BTSC stereo signal to be passed throughout the house via coaxial cable, avoiding the high cost, poor stereo separation, and low noise immunity of unbalanced RCA cables. This simplified approach can be used because the vestigial 15.734-kHz pilot signal in the BTSC composite audio spectrum provides an ideal reference signal to the phase detector of the PLL.

The RF outputs of *cable* TV set-top boxes (modulated on Channel 3 or Channel 4) are already BTSC stereo encoded. However, the RCA outputs of inexpensive *satellite* TV set-top boxes are often limited to monophonic sound. To add stereo capability to a satellite STB, an AD71028 BTSC stereo encoder is added to the system. In homes with multiple TVs, an ADC is required in the primary satellite STB to convert the left- and right analog audio signals to digital before encoding. A master clock is required for the AD71028, the ADC, and other professional audio converters and components. These components have a quasi-standard sample rate of 48 kHz, but are typically oversampled at 12.288 MHz (48 kHz × 256). With a 12.288-MHz master clock and digitized L and R audio channels, the encoder will generate the main monaural channel (L + R), the BTSC stereo subchannel (L – R), and the 15.734-kHz pilot signal.

The master clock, which, in turn, generates a fractionally proportional pilot signal, can be generated in one of several ways. One option, the use of a crystal-based oscillator, will not ensure that the corresponding BTSC pilot signal is frequency- or phase-locked to f_{Hsync}, a requirement to accurately decode the double-sideband suppressed-carrier-encoded stereo audio. At the remote television, video signals can be as much as 10 dB higher than the audio, potentially causing phase alignment errors in the stereo matrix decoding. In addition, even the best available highly stable crystals are only specified to 0.01%, corresponding to a 1.6 Hz tolerance in the pilot signal. For example, if the PLL in the BTSC receiver were to lock onto a strong artifact of the NTSC f_{Hsync}, instead of the crystal-generated pilot, the signal differences will result in time-varying phase misalignment between L + R and L – R, causing a severe loss of separation between the left and right channels during decode. Also, depending on the architecture of the phase detector, the VCO may vacillate between the crystal-generated pilot and the f_{Hsync} artifact, again resulting in phase misalignment.

A more viable option is to derive a clock with a fractional-N PLL, actually using the f_{Hsync} as a reference input. Figure 5 shows a typical PLL with a fractional-N divider in its feedback path. If f_{Hsync} is used as the input reference, the value of the N divider is 780.9838... ($N = f_{MCLK}/f_{Hsync}$) requiring a very high resolution device. This approach also requires additional components, making it impractical in designs where board space is at a premium.

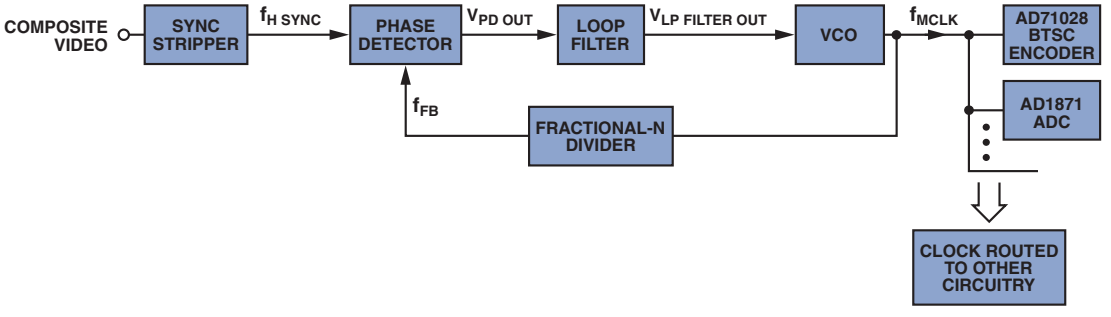

Figure 5. Typical MCLK derivation using a PLL. The fractional-N divider is set so that MCLK is 12.288 MHz.

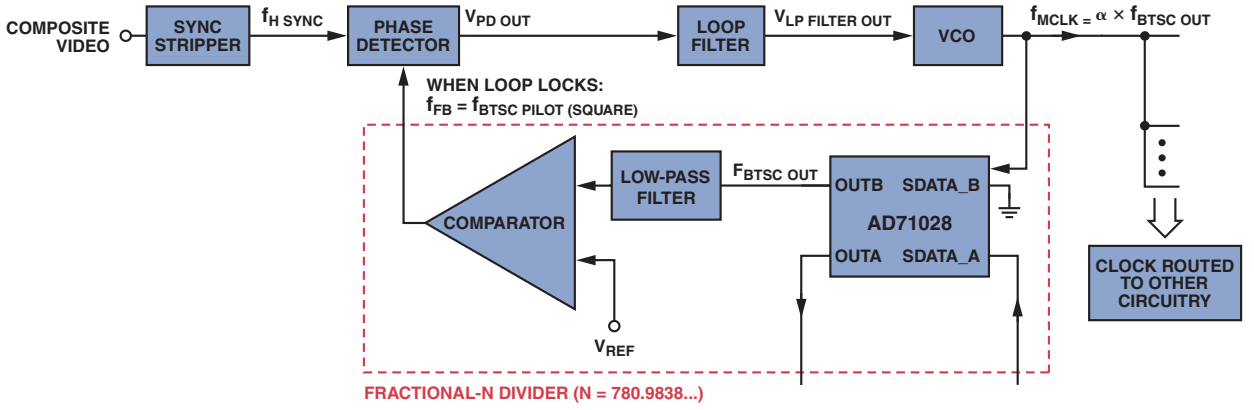

Figure 6. f_{MCLK} synthesis with H-sync and BTSC pilot. Observe how the AD71028 is incorporated in the feedback loop of the PLL.

A third option is to include the secondary channel of the AD71028—which contains two stereo audio channels—in the feedback loop, using it to self-correct and self-sustain the master clock—as shown in Figure 6. The primary (A) channel of the AD71028 is used for encoding BTSC stereo audio. It receives its digital inputs from an audio ADC, such as the AD1871. If the audio inputs of the secondary (B) channel are grounded, only the vestigial pilot is seen at the output. If phase- and frequency-locked to f_{Hsync}, this signal can be used to generate the 12.288-MHz master clock, f_{MCLK}.

After the B-channel output of the encoder, a two-pole, low-pass filter and a biased comparator are needed to provide a clean square wave pilot signal to the phase detector. Any errors in the AD71028's master-clock frequency will be reflected immediately through the secondary channel to the phase detector's feedback input via the vestigial pilot, which is directly proportional to f_{MCLK}. Thus, this BTSC pilot feedback clock-synthesis method will provide a more accurate master clock than a conventional fractional-N PLL clock, since the master clock will be generated directly with the correct frequency feedback ratio. In this application, the PLL concept is successful because the AD71028 core is able to generate the pilot tone digitally at a fixed fractional ratio to the f_{MCLK}.

Thus, the master clock frequency must be precisely 12.288 MHz for the pilot tone to be 15.734 kHz. When the loop settles and locks, f_{MCLK} will be a fractional multiple of the instantaneous frequency of the BTSC encoder output, $f_{btsc\ out}$ (that is, $f_{MCLK} = \alpha \times f_{btsc\ out}$), and the pilot sent to the remote television is locked to the NTSC f_{Hsync}. Coupled artifacts of f_{Hsync} at the receiver are identical in phase and frequency to the pilot, so there is no erroneous demodulation.

When two TVs are connected to one satellite STB using a simple STB, the TV in a distant room must be connected via coaxial cable. The satellite dish is connected directly to the STB, via ANT IN, as shown in Figure 7. The audio signal is routed to the main TV via RCA cables, and the second TV receives its audio and video on Channel 3 or 4 via coaxial cable. The second TV will receive only monophonic sound, though, because the stereo difference signal, L – R, is not present in the audio spectrum it receives (Figure 8).

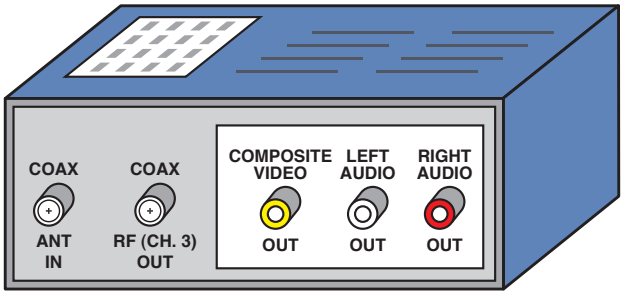

Figure 7. A/V inputs and outputs of a satellite STB.

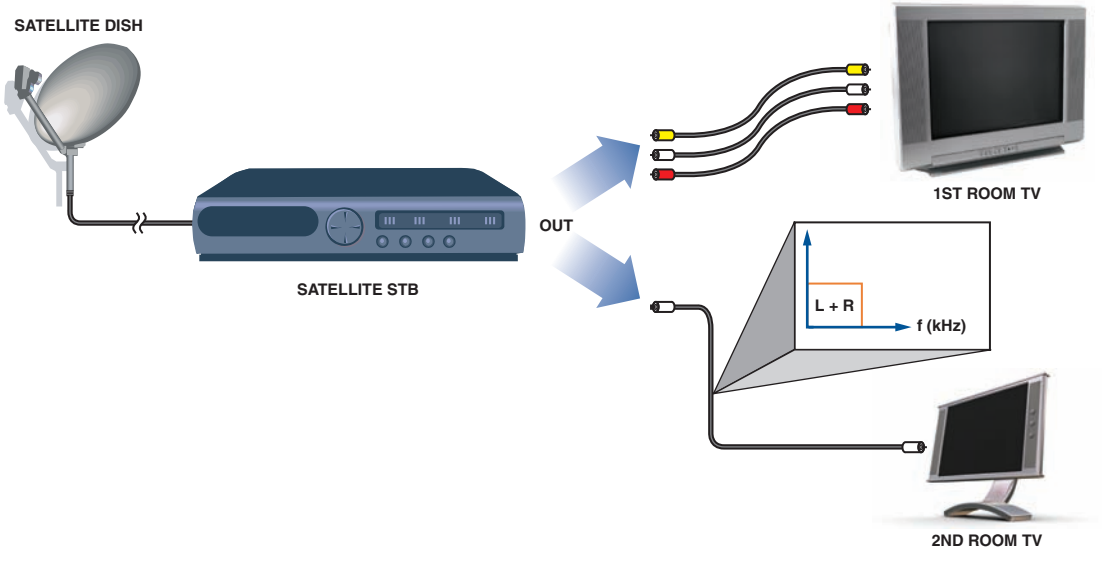

Figure 8. Audio spectrum of typical satellite TV setup where monaural audio is sent to 2nd room TV.

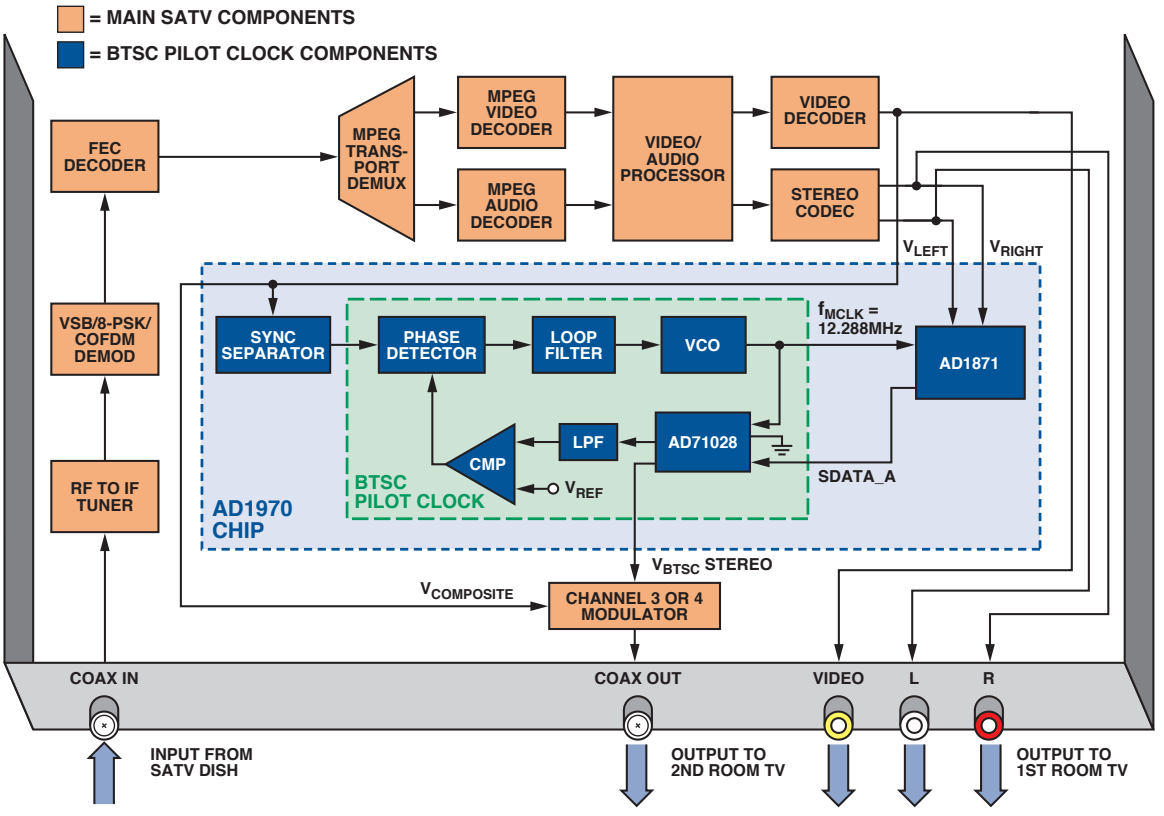

Figure 9. Block diagram of SATV receiver. MCLK is derived using a BTSC pilot. The AD71028's A channel output can be used to provide BTSC stereo to a second room TV or secondary A/V receivers.

The reason for this is that BTSC encoders have traditionally been expensive because designs require many analog components, a large board space, and complex calibration adjustments, making them impractical for low-cost satellite STBs. If one desires to preserve stereo sound in such a system, the decoded left and right analog audio signals must be passed to the second (remote) TV via extended unbalanced RCA cables, paralleled with the L and R cables shown in Figure 8, but this setup is highly susceptible to noise and signal degradation.

If, on the other hand, the AD71028, a dual-channel BTSC stereo encoder, is used as described above, its A channel can be used for passing encoded video and stereo audio to a second TV via a single coaxial cable. In homes where TVs and audio/video receivers may be in multiple rooms, the consumer can now pass BTSC stereo throughout the house via coaxial cable.

Figure 9 shows a block diagram of a *satellite-access-TV* (SATV) receiver. It has an RF output with BTSC stereo and a PLL-generated MCLK.

Digital BTSC Encoder Including ADC

The recently released AD1970[2] incorporates the AD71028[1] BTSC encoder and the AD1871[3] ADC. The required inputs to this device are the NTSC composite video signal and L and R audio channels. Since the clock is self-generated with the concealed secondary channel in the core, no external clock is needed to drive this part. The AD1970 thus offers a fully integrated solution for BTSC-enabled satellite STB applications.

CONCLUSION

A novel application of a phase-locked loop provides an accurate, low-drift, self-correcting master clock for satellite set-top boxes. A BTSC pilot from the secondary channel of a dual BTSC encoder is continuously compared with the NTSC horizontal sync rate (15.734 kHz) to derive a self-sustaining stable master clock frequency of 12.288 MHz. This clock can be routed to other professional audio converters and components, and it can be used as a source for deriving further clock frequencies. In addition, the primary channel of the encoder provides a BTSC stereo-encoded output. This allows secondary TVs and A/V receivers to be interconnected via single standard coaxial cables. In TV and A/V setups where devices are far apart, this approach maintains the signal integrity of the system cost-effectively.

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[3]ADI website: www.analog.com (Search) AD1871 (Go)

This article can be found at http://www.analog.com/library/analogdialogue/archives/39-07/btsc.html, with a link to a PDF.

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